**AMENDMENTS TO THE CLAIMS**

**(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)**

Please cancel claims 1 and 22-28 without prejudice.

1. (CANCELED)

2. (PREVIOUSLY PRESENTED) An apparatus comprising:

a first set state machine configured to generate a first set-output signal that is either at a first logic state or at a second logic state in response to (i) a first read clock, (ii) a first write clock, (iii) a first programmable almost full look-ahead signal and (iv) a first control signal;

a second set state machine configured to generate a second set-output signal that is either at said first logic state or at said second logic state in response to (i) a second read clock, (ii) a second write clock, (iii) a second programmable almost full look-ahead signal and (iv) a second control signal;

a synchronizer configured to generate a synchronized output signal in response to said second set-output signal and a reset signal;

a latch configured to generate (i) a first latch output signal in response to said first set-output signal and said synchronized output signal and (ii) a second latch output signal as a complement of said first latch-output signal, said first latch

output signal representing an almost full output flag that is at said first logic state when a FIFO (First In First Out) memory block is almost full, and is at said second logic state when said FIFO is not almost full;

a first logic block configured to generate said first control signal in response to said second latch output signal; and

a second logic block configured to generate (i) said reset signal and (ii) said second control signal in response to said first latch output signal.

3. (PREVIOUSLY PRESENTED) The apparatus of claim 2, wherein said synchronizer comprises:

a SR latch configured to time said second set-output signal depending on said reset signal; and

a Flip-Flop (FF) block configured to generate said synchronized signal depending on (i) an external timing signal and (ii) said second set-output signal as timed by said SR latch.

4. (PREVIOUSLY PRESENTED) The apparatus of claim 3, wherein said external timing signal comprises:

a free running write clock signal.

5. (ORIGINAL) The apparatus of claim 2, wherein said FIFO comprises:

a synchronous FIFO.

6. (PREVIOUSLY PRESENTED) The apparatus of claim 2, wherein said first write clock comprises:

a first enabled write clock.

7. (PREVIOUSLY PRESENTED) The apparatus of claim 2, wherein said first read clock comprises:

a first enabled read clock.

8. (PREVIOUSLY PRESENTED) The apparatus of claim 2, wherein said second write clock comprises:

a second enabled write clock.

9. (PREVIOUSLY PRESENTED) The apparatus of claim 2, wherein said second read clock comprises:

a second enabled read clock.

10. (PREVIOUSLY PRESENTED) The apparatus of claim 2 further comprising:

a first delay block configured to increase a first pulse width of said first latch output signal before said second logic block.

11. (PREVIOUSLY PRESENTED) The apparatus of claim 10 further comprising:

a second delay block configured to increase a second pulse width of said second latch output signal before said first logic block.

12. (PREVIOUSLY PRESENTED) The apparatus of claim 10, wherein said first delay block has a predetermined delay configured during fabrication.

13. (PREVIOUSLY PRESENTED) The apparatus of claim 10, wherein said first delay block comprises:

a programmable delay block configured to change said first pulse width.

14. (PREVIOUSLY PRESENTED) The apparatus of claim 10, wherein said first delay block comprises:

a programmable delay block responsive to an externally generated signal.

15. (PREVIOUSLY PRESENTED) The apparatus of claim 14, wherein said programmable delay block comprises:

a joint test access group (JTAG) programmable delay block.

16. (PREVIOUSLY PRESENTED) The apparatus of claim 15, wherein a set of additional JTAG instructions are utilized to program said JTAG programmable delay block.

17. (PREVIOUSLY PRESENTED) The apparatus of claim 11, wherein said second delay block has a second predetermined delay configured during fabrication.

18. (PREVIOUSLY PRESENTED) The apparatus of claim 11, wherein said second delay block comprises:

a programmable delay block configured to change said second pulse width.

19. (PREVIOUSLY PRESENTED) The apparatus of claim 11, wherein said second delay block comprises:

a programmable delay block responsive to an externally generated signal.

20. (PREVIOUSLY PRESENTED) The apparatus of claim 19, wherein said programmable delay block further comprises:

a joint test access group (JTAG) programmable delay block.

21. (PREVIOUSLY PRESENTED) The apparatus of claim 20, wherein a set of additional JTAG instructions are utilized to program said JTAG programmable delay block.

22. (PREVIOUSLY PRESENTED/CANCEL) A method for determining an almost emptiness of at least one memory buffer, comprising the steps of:

(A) generating an almost full output flag in response to (i) a first read clock, (ii) a first write clock, (iii) a first programmable almost full look-ahead signal, (iv) a second read clock, (v) a second write clock (vi) and a second programmable almost full look-ahead signal;

(B) generating a not almost full output flag as a complement of said almost full output flag; and

(C) presenting said first read clock, said first write clock, said first programmable almost full look-ahead signal, said second read clock, said second write clock and said second programmable almost full look-ahead signal to a state machine, wherein said state machine generates said almost full output flag and said not almost full output flag.

23. (CANCELED)

24. (CANCELED)

25. (CANCELED)

26. (CANCELED)

27. (CANCELED)

28. (CANCELED)

29. (CURRENTLY AMENDED) An apparatus comprising:

means for generating a first output signal either at a first logic state or at a second logic state in response to (i) a first read clock, (ii) a first write clock, (iii) a first programmable almost full look-ahead signal and (iv) a first control signal;

means for generating a second output signal either at said first logic state or at said second logic state in response to (i) a second read clock, (ii) a second write clock, (iii) a second programmable almost full look-ahead signal and (iv) a second control signal;

means for generating a synchronized output signal in response to (i) said second output signal and (ii) a reset signal;

means for generating (i) a first latch output signal representing an almost full output flag that is at a first logic state when a FIFO memory block is almost full and is at a second logic state when said FIFO is not almost full, in response to said first output signal and said synchronized output signal and (ii) a second latch output signal as a complement of said first latch output signal;

means for generating said first control signal in response to said second latch output signal; and

means for generating (i) said second control signal and (ii) said reset signal in response to said first latch output signal.

30. (PREVIOUSLY PRESENTED) The apparatus of claim 29 further comprising:

means for increasing a pulse width of said first latch output signal.

31. (PREVIOUSLY PRESENTED) The apparatus of claim 29 further comprising:

means for increasing a pulse width of said second latch output signal.